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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,725	12/28/2000	James S. Burns	2207/10120	6772

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EXAMINER	
CHAN, EDDIE P	

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,725	BURNS ET AL.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/28/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of the following papers:

1) Ext. of Time (4/12/04)

2) Amendment A (4/12/04)

These papers have been placed of record in the file.

2. Claims 1, 2, 4-8, 10-15, 17, and 18 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1, 2, 4-6 and 13-15, 17, and 18** are rejected under 35 U.S.C. 102(b) as being anticipated by Hirata et al (US005430851A).

5. In regard to claim 1:

6. Hirata et al. disclose a processor (col. 4, line 50), comprising,

7. a plurality of pipelined functional units for executing instructions (Fig. 3, elements 16-18);

8. a scheduler (Fig. 4, instruction setup units 34 and instruction schedule unit 35 [col. 9, lines 36-45]), coupled to the plurality of functional units (fig. 4, 16-18), programmed for independently mapping instructions, received from at least two separate instruction groups, to at least a portion of the functional units (independent instruction setup units for each instruction stream [col. 5, lines 55-59] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]) during a first stage (fig. 4, instruction setup units 34 comprise of the first stage).

9. wherein the scheduler is programmed to merge (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remap (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) a plurality of instruction subgroups, each subgroup from a respective separate instruction group (col. 9, lines 46-64: the instruction schedule unit 35 receives an instruction subgroup of up to 2 instructions from the instruction stream being fetched), to at least a portion of the functional units, based on functional unit requirements and availability (signal R, col. 6, lines 54-56), during a second stage (fig. 4, instruction schedule unit 35 comprises of a second stage).

10. In regard to claim 2:

11. Hirata et al. further disclose that the scheduler is programmed to deliver the instruction to the portion of functional units following merging and remapping

(instructions are sent to the functional units from the instruction schedule unit 35 which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

12. In regard to claim 4:

13. Hirata et al. further disclose that the functional units execute an increased number of instructions operating at a given clock rate (col. 2, lines 61-64).

14. In regard to claim 5:

15. Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

16. In regard to claim 6:

17. Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

18. In regard to claim 13:

19. Hirata et al. disclose a method of dispersing instructions (instruction schedule unit distributes instructions to the functional units, col. 6, lines11-14) to be executed by a processor (col. 4, line 50), comprising:

20. mapping instructions (instruction setup units [fig. 4, 34] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]), received from at

least two separate, independent instruction groups (instruction streams, col. 5, lines 55-59), to at least a portion of a plurality of pipelined functional units during a first stage (instruction setup unit 34);

21. merging (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remapping (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) a plurality of instruction subgroups, each subgroup from a respective separate instruction group (col. 9, lines 46-64: the instruction schedule unit 35 receives an instruction subgroup of up to 2 instructions from the instruction stream being fetched), to at least a portion of functional units, based on functional unit requirements and availability (signal R, col. 6, lines 54-56), during a second stage (instruction schedule unit 15).

22. In regard to claim 14:

23. Hirata et al. further disclose the step of delivering the instructions to portions of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

24. In regard to claim 15:

25. Hirata et al. further disclose that the step of merging and remapping includes merging and remapping the instructions to the portion of functional units to allow

execution of an increased number of instructions at a given clock rate (col. 2, lines 61-64).

26. In regard to claim 17:

27. Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

28. In regard to claim 18:

29. Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made*

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims **7, 8, 10-12** are rejected under 35 U.S.C. 103(a) for the same reasons as claims 1, 2, 4-6 above as being unpatentable over Hirata et al. (US005430851A) in view of Tannenbaum ("Structured Computer Organization," Prentice-Hall, 1984, pp. 10-12).

32. Hirata et al. differs from the applicant's invention in that it does not teach that instructions on a machine-readable medium comprise instructions for performing the limitations of claims 1-6 of the applicant's invention.

33. However Tannenbaum teaches that any instruction executed by hardware can also be simulated in software (pg 11, para. 4, lines 1-2).

34. One of ordinary skill in the art at the time of the invention would have converted the Hirata et al. reference to software i.e. instructions on a machine readable medium from the teachings of Tannebaum.

35. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Hirata et al. processor by converting it to instructions on a machine-readable medium.

Response to Arguments

36. Applicant's arguments with respect to claims 1, 2, 4-8, 10-15, 17, and 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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